DOCTORAL CANDIDATE:	Christian Ferdinand Beckhoff
DEGREE:	Doctor Philosophiae
FACULTY:	Faculty of Mathematics and Natural Sciences
DEPARTMENT:	Department of Informaitcs
AREA OF EXPERTISE:	Design Tools for Reconfigurable Systems
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DISSERTATION TITLE: GOAHEAD - *A Framework for Building Reconfigurable Systems*

For more than two decades, partial reconfiguration on FPGAs has been investigated intensively in academia. The benefits of partial reconfiguration are widely accepted, and the two main FPGA vendors Xilinx and Altera provide commercial tools for building reconfigurable systems. However, a widespread commercial use of partial reconfiguration has not yet appeared.

This is mainly caused by a lack of adequate design tools. On the one hand, building reconfigurable systems is still an expert's domain, as one has to cope with many low-level FPGA architecture details. On the other hand, the currently available tools do not allow building flexible and resource efficient reconfigurable systems. The lack of adequate design tools prevents the exploitation of the capabilities of partial reconfiguration, and moreover, is the motivation for this thesis.

In this thesis, an automated tool flow for building reconfigurable system was developed that overcomes many limitations of existing tools for partial reconfiguration. This tool flow comprises novel algorithms for floorplanning reconfigurable systems, resource efficient interface implementations, and flexible module relocation. Various design rule checks verify the correct implementation of the static system and the reconfigurable modules. A strict encapsulation of the static system and the reconfigurable modules allows changes in one of the latter without affecting the other. Moreover, GOAHEAD enables a component based design flow by providing means for composing complete systems out of physically pre-implemented modules. GOAHEAD allows modules with bus interfaces and streaming connections that can be arbitrarily relocated or stitched together to processing pipelines.
Due to its high degree of automation, GOAHEAD can rapidly compile different design parameters into bitstreams allowing for a design space exploration. GOAHEAD supports all recent Xilinx FPGAs and is designed in a way that future devices will also be supported.
Furthermore, GOAHEAD provides a user friendly GUI or can alternatively be controlled through a powerful scripting interface that allows building complete systems in batch mode.

GOAHEAD has proved its maturity in different research projects that will be introduced throughout the thesis. The tool, example systems, and tutorials are available on the COSRECOS website.