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In this thesis, we develop an improved power modelling methodology for the Tegra K1 System-on-Chip, a mobile multiprocessor. Our model predicts the power usage of the Tegra K1 with an accuracy close to 100 %, and exposes detailed insight into how different mobile applications consume energy across the many heterogeneous processor cores and memories of the Tegra K1. This is a substantial improvement over existing methods. Due to our model's high level of detail, it provides valuable insight into how the design choices of system architects and developers impact the energy consumption of the chip at a fine-grained level. This enables software engineers to code more energy-efficient applications and manage chip temperature. For example, by reducing the clock frequency of the different processor cores and memory, we have achieved up to 30 % reduced energy consumption compared to the standard frequency scaling algorithms. This corresponds to the same increase in battery lifetime. Furthermore, we demonstrate an additional 35 % improvement by utilizing the appropriate processor cores for specific applications, as well as additional energy savings of 3.2 % and 50 % when lowering precision, utilizing special, non-coherent caches and special multimedia processing instructions.